IN THE DRAWINGS

With the concurrence of the Examiner, applicants propose to amend the drawings by labeling Figure 1 as prior art in accordance with the red ink notation on the accompanying copy of Figure 1.

REMARKS

On page 3 of the Office Action, the Examiner required amendment of Figure 1 of the drawings. Accordingly, Figure 1 is being amended to comply with the Examiner's requirement.

On pages 4-6 of the Office Action, the Examiner rejected claims 1-6 under 35 U.S.C. §102(e) as being anticipated by the Huai patent.

The Huai patent discloses magnetic elements 1 and 1' that may be used as memory elements. The element 1 is a spin valve 1 and includes an antiferromagnetic layer 2, a pinned layer 4, a spacer layer 6, and a free layer 8. The pinned layer 4 and the free layer 8 are ferromagnetic. The spacer layer 6 is nonmagnetic and conductive. The antiferromagnetic layer 2 fixes, i.e., pins, the magnetization of the pinned layer 4 in a particular fixed direction. The magnetization of the free layer 8 is free to rotate, typically in response to an external field.

The magnetic element 1' is a spin tunneling junction and includes an antiferromagnetic layer 2', a pinned layer 4', an insulating barrier layer 6' and a free layer 8'. The barrier layer 6' is thin enough for

electrons to tunnel through in a spin tunneling junction 1'.

When the magnetizations of the free layer 8/8' and the pinned layer 4/4' are parallel, the resistance of the device 1/1' is low. When the magnetizations of the free layer 8/8' and the pinned layer 4/4' are antiparallel, the resistance of the device 1/1' is high. In order to sense the resistance of the magnetic element 1/1', current is driven through the magnetic element 1/1' in a direction that is either parallel or perpendicular to the layers.

Figure 2 depicts a memory array 10 using four memory cells 20 each of which includes the device 1' and a transistor 22. The memory cells 20 are coupled to a reading/writing column selector 30 via bit lines 32 and 34 and to a row selector 50 via word lines 52 and 54. Write lines 60 and 62 carry currents during writing. The reading/writing column selector 30 is coupled to a write current source 42 and a read current source 40.

In order to write to the memory array 10, the write current source 42 is applied to the bit line 32 or 34 as selected by the reading/writing column selector 30, the read current source 40 is not applied, both word lines 52 and 54 are disabled, and the transistors 22 are

disabled. In addition, one of the write lines 60 and 62 is selected to carry a write current to the selected memory cell 20. The combination of the current in the write line 60 or 62 and the current in the bit line 32 or 34 generates a magnetic field large enough to switch the direction of magnetization of the free layer 8' and thus write to the desired memory cell 20. Depending upon the data written to the selected memory cell 20, the device 1' will have a high resistance or a low resistance.

When reading from the memory cell 20, the read current source 40 is applied. The memory cell 20 selected to be read is determined by the row selector 50 and by the reading/writing column selector 30. The output voltage is read at the output line 44. This output voltage has a value dependent upon the resistance of the selected memory cell 20 which, in turn, is determined by the value of the data stored in that memory cell 20.

According to the Huai patent, there are barriers to the use of the element 1' and the magnetic memory cell 20 at higher memory cell densities because the magnetic field that is required to switch the magnetization of the free layer 8' is inversely proportional to the width of the element 1'. As a

result, the current required to be driven through the bit line 32 or 34 and particularly through the write line 60 or 62 increases dramatically for higher magnetic memory cell density. This large current can result in increased cross talk and power consumption. In addition, the driving circuits required to drive the current that generates the switching field at the desired memory cell 20 also increase in area and complexity. Furthermore, the write currents have to be large enough to switch the selected memory cell 20 but not so large that the neighboring cells are inadvertently switched.

The Huai patent purports to overcome these barriers by using a spin-polarized current to switch the magnetization direction of the free layer as long as the free layer is sufficiently thin, i.e., preferably less than 10 nm. Accordingly, the magnetization of the free layer 8 in the spin valve 1 is switched using spin transfer by driving a current from the free layer 8 to the pinned layer 4 or by driving current from the pinned layer 4 to the free layer 8.

The Huai patent further states that, although the phenomenon of spin transfer can be used to switch the direction of the magnetization of the free layer 8/8', there are additional barriers to using the element 1/1'

in the memory cell 20. For example, the magnetoresistance ratio of the spin valve 1 is only approximately two percent. In addition, because the total resistance of the spin valve 1 is low, the read signal output by the spin valve 1 is very low. A high current density is required to induce the spin-transfer effect in the spin tunneling junction 1' that could destroy the thin insulating barrier. Moreover, the spin transfer has not been observed in the spin tunneling junction 1' at room temperature.

The Huai patent purports to solve these problems by providing a magnetic element 100 that includes a first pinned layer 104, a nonmagnetic spacer layer 106, a free layer 108, a barrier layer 110, and a second pinned layer 112. The first and second pinned layers 104 and 112 and the free layer 108 are ferromagnetic. The first pinned layer 104 has a magnetization pinned in a first direction by an antiferromagnetic layer 102, and the second pinned layer 112 has a magnetization pinned in a second direction by an antiferromagnetic layer 114. The first and second directions may be the same direction or opposite directions. The magnetization of the free layer 108 is

allowed to change direction due to spin transfer when a write current is passed through the magnetic element 100.

The magnetic element 100 can be considered to be a combination of a spin valve and a spin tunneling junction. The spin valve includes the first antiferromagnetic layer 102, the first pinned layer 104, the conductive spacer layer 106, and the free layer 108, and the spin tunneling junction includes the free layer 108, the insulating barrier layer 110, the second pinned layer 112 and the second antiferromagnetic layer 114. The spin valve portion of the magnetic element 100 writes to the free layer 108 using spin transfer, and the spin tunneling portion of the magnetic element 100 reads the magnetic element 100.

The free layer 108 has a thickness of less than or equal to 10 nm.

Independent claim 1 is directed to a giant magnetoresistive memory device that includes a magnetic storage layer, a magnetic sense layer, a non-magnetic spacer layer between the magnetic sense layer and the magnetic storage layer, and an antiferromagnetic layer formed in proximity to the magnetic storage layer whereby the antiferromagnetic layer couples magnetically in a controlled manner to the magnetic storage layer such that

the magnetic storage layer has uniform and/or directional magnetization.

The Huai patent does not disclose a memory device that has both a storage layer and a sense layer. The memory device disclosed in the Huai patent has only the free layer 108. The magnetization of the magnetic layer 104 is pinned and, therefore, cannot act as either a storage layer or a sense layer.

Accordingly, independent claim 1 is not anticipated by the Huai patent.

Because independent claim 1 is not anticipated by the Huai patent, dependent claim 2-6 are not anticipated by the Huai patent.

On pages 6 and 7 of the Office Action, the Examiner rejected claims 1 and 7-9 under 35 U.S.C. §102(b) as being anticipated by the Maruyama patent.

The Maruyama patent discloses in Figure 1D a reproducing (i.e., reading) magnetic head that is used to read data from a storage device. Accordingly, the magnetic head of Figure 1D is not a memory device. The actual memory device as disclosed in the Maruyama patent is the recording medium (or disk) 11. The magnetic head disclosed in Figure 1D is used to read data from the memory device 11.

Specifically, the magnetic head shown in Figure 1D includes a magnetoresistive element 32 and electrodes 31. A giant magnetoresistive element can be used as the magnetoresistive element 32. Specifically, the magnetoresistive element 32 includes a first giant magnetoresistive element 33 and a second giant magnetoresistive element 34 with a non-magnetic film 36 therebeween . Permanent magnets 35 are provided on both ends of the giant magnetoresistive elements 33 and 34 to change the soft magnetic layer which is a component of the giant magnetoresistive element to a single domain and to arrange magnetization in the same direction.

The giant magnetoresistive element 34 includes a matching material layer 41, a ferromagnetic free layer 42, a spacer 43, a pinned layer 44, and an antiferromagnetic layer 45 to fix the magnetization layer of the pinned layer 44. The giant magnetoresistive element 33 includes a matching material layer 46, a ferromagnetic free layer 47, a spacer 48, a pinned layer 49, and an antiferromagnetic layer 50 to fix the magnetization layer of the pinned layer 44.

As shown in Figure 1D, the magnetization direction of the pinned layer 44 is opposite to the magnetization direction of the pinned layer 49.

Because the magnetic head of Figure 1D is used to read data from the recording medium 11, both of the ferromagnetic layers 42 and 47 are sense layers. Thus, the magnetic head of Figure 1D has no storage layer.

As can be seen, the device shown in Figure 1D of the Maruyama patent is not a memory device. It is a magnetic head that is used to read data from a memory device 11.

Accordingly, the Maruyama patent does not anticipate independent claim 1 which is directed to a memory device having a storage layer.

Moreover, the magnetic head shown in Figure 1D of the Maruyama patent has no storage layer. Its layers are either sense layers or are pinned.

For this reason also, the Maruyama patent does not anticipate independent claim 1 which is directed to a memory device having a storage layer.

Because independent claim 1 is not anticipated by the Maruyama patent, dependent claim 7-9 are not anticipated by the Maruyama patent.

On pages 7-9 of the Office Action, the Examiner rejected claims 13-23 under 35 U.S.C. §102(e) as being anticipated by the Lin published application.

The Lin published application also discloses a reading head for reading information from a memory device 312. Specifically, as shown in Figure 3, a disk drive 300 includes the memory device (disk) 312 which is supported on a spindle 314 and is rotated by a drive motor 318. A slider 313 is positioned on the memory device 312 and supports a read/write head 321 that incorporates a dual spin valve sensor 600 which is the subject of the Lin published application. The slider 313 is attached to an actuator arm 319 by a suspension 315. The actuator arm 319 is attached to an actuator 327 controlled by current signals from a controller 329. Read and write signals are communicated to and from the read/write head 321 through a channel 325.

Figures 4 and 5 show heads that can be used for the read/write head 321.

Figure 6 of the Lin published application shows the dual spin valve sensor 600 that includes end regions 604 and 606 separated from each other by a central region 602.

A first spin valve stack 608 is deposited over a seed layer 614 and includes an antiferromagnetic layer 616, a pinned layer 617, a spacer layer 624, and a sense layer 625. The pinned layer 617 is formed of two

ferromagnetic layers 618 and 622 separated by an antiparallel nonmagnetic coupling layer 620.

A bias stack 610 is deposited over the first spin valve stack 608 and includes a decoupling layer 629, a ferromagnetic layer 630, an antiferromagnetic layer 632, a ferromagnetic layer 634, and a second decoupling layer 633.

A spin valve stack 612 is deposited over the bias stack 610 and includes a sense layer 639, a spacer layer 640, a pinned layer 641, and an antiferromagnetic layer 648. The pinned layer 641 is formed of two ferromagnetic layers 642 and 646 separated by an antiparallel nonmagnetic coupling layer 644.

The sense layer 625 has a magnetization 627 that is free to rotate in the presence of a signal magnetic field. The sense layer 639 has a magnetization 637 that is also free to rotate in the presence of a signal magnetic field. The antiferromagnetic layer 632 pins the magnetizations 631 and 635 of the ferromagnetic layers 630 and 634, respectively. The magnetizations 631 and 635 of the ferromagnetic layers 630 and 634 provide longitudinal bias fields which form flux closures with the sense layers 625 and 639, respectively, to stabilize the sense layers 625 and 639.

Because the dual spin valve sensor 600 of the Lin published application is used to read data from the recording medium 312, both of the ferromagnetic layers 625 and 639 are sense layers. Thus, the dual spin valve sensor 600 of the Lin published application has no storage layer.

As can be seen, the dual spin valve sensor 600 of the Lin published application is not a memory device. It is a magnetic head that is used to read data from the memory device 312.

Accordingly, the Lin published application does not anticipate independent claim 13 which is directed to a memory device having a storage layer.

Moreover, the dual spin valve sensor 600 of the Lin published application has no storage layer. Its layers are either sense layers or are pinned.

For this reason also, the Lin published application does not anticipate independent claim 13 which is directed to a memory device having a storage layer.

Because independent claim 13 is not anticipated by the Lin published application, dependent claim 14-23 are not anticipated by the Lin published application.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

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